**CS3220 Spring 2017**

**Assignment #2 (10 points): Due March 13 (Monday) 6 pm.**

In this assignment you will design a multi-cycle processor. Please see 7.lec\_isa.pptx for the ISA specification and 8 .lec\_multicycle.pptx for the processor design description. You will design your own processor although you can follow the similar design as in lec\_multicycle.pptx.

You should demonstrate that your processor can execute the provided test assembly code correctly and also your own version of fmedian.mif file. The outcomes of HEX will be used to check correctness.

[1] Write an assembler. We provide test.asm and test.mif to initialize the instruction memory until you build your own assembler. You can choose any programming language to design your assembler.

[2] Design the processor that works test.mif.

[3] Write an assembly code that find a median value in a given array. You use the same array values in the provided test.asm. Your assembly code (fmedian.asm) should produce your own version of “fmedian.mif”.

We provide assignment2\_frame.qar to help you start. You should submit all the files in the assignment2.qar including your own fmedian.mif.

Your code should be executed in less than 120 sec. If your code runs much quicker (i.e. less than 30 sec), your design is probably wrong.

What to submit:

[1] assignment2.qar (including fmedian.mif and all other files).

You and your partner should submit the same version of qar file.

Please download your submitted file and verify whether your qar file contains all the files and runs correctly. It must contain fmedian.mif. We will download your qar file to grade and if you are missing fmedian.mif you will lose 25% and if your verilog design is missing and won’t compile, we will contact you to get missing files but each time we contact you, you will lose 10%.

Your design should run less than 120 sec and display the correct value.

[2] Report: You must submit your **own version** of your report. (**Report.pdf**) Your should write a report independently (your partner will write his/her own report) and submit it. The report should include

- Design options and approaches that you have taken

- Problems/issues and how you solved

- Processor design diagram and state machines (including state number and control signals). These diagrams can be shared with your partner.

- Contribution to the project.: What you have done and what percentage your contribution is.

Your report might be 1 page excluding diagrams.

Your grade = (correctness\_score)\*(0.5 + (the quality of the report))

The quality of the report will vary from 0.4 – 0.5.

***Please do not procrastinate.*** You will not get any credit if your design does not produce the final value. And if you don’t have a working assignment #2, you will not be able to continue the rest of the project. Both test.mif and fmedian.mif should show the correct outcomes in order to get a full credit.